**MILLER COMPENSATED TWO-STAGE OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA) CONFIGURATION (SIMULATION PROJECT)**

A S Gouthami  
dept. of electronics and communication engineering  
The national institute of engineeringMysore, India  
l[2023ec\_asgouthami\_a@nie.ac.in](mailto:2023ec_asgouthami_a@nie.ac.in)

B P Sapthami   
 *dpt.*  of electronics and communication engineering  
The national institute of engineering Mysore, India  
 2023ec\_bpsapthami\_a@nie.ac.in

Abstract— This project involves the design and LTspice simulation of a Miller-compensated two-stage operational transconductance amplifier (OTA) using 180nm CMOS technology. The architecture consists of a differential input stage followed by a common-source gain stage, with Miller compensation applied to ensure stability and achieve an adequate phase margin for closed-loop operation .

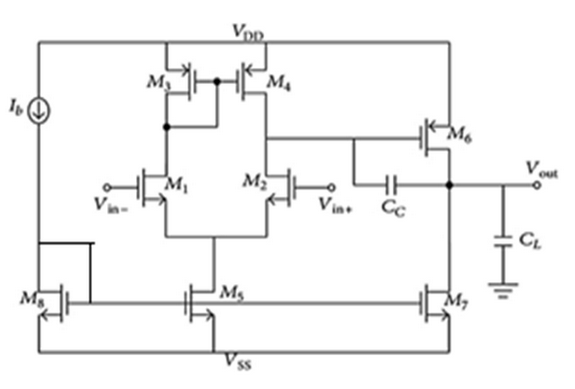
Technical details: The Miller-compensated two-stage OTA is designed and simulated in LTspice using a 2 V supply with a total bias current of 100 μA,

# Introduction

Operational Transconductance Amplifiers (OTAs) are a class of amplifiers where the output current is proportional to the differential input voltage, making them essential in analog signal processing. Among various OTA architectures, the two-stage OTA is widely used due to its high gain and wide output swing.

The Miller-compensated two-stage OTA offers a high open-loop gain and improved output voltage swing, making it suitable for low-frequency and precision analog applications. This configuration allows the OTA to drive capacitive loads efficiently and maintain consistent performance across a wide range of operating conditions. Additionally, it provides good common-mode rejection and power efficiency, which are crucial in low-power and high-performance analog circuit design.

# Circuit diagram



# **Design Specification**

DC gain = 70dB, GB = ~5MHz, Phase margin>= 600, Slew rate = 10uV/s, Cc= 3pF, CL= 10pF, (UnCox)n = 280uA/V2,

(UnCox)p = 160uA/V2, VSS= -2.5V, VDD=2.5V Power<1mW, L= 500nm,

Iref = 30uA.

# CIRCUIT ANALYSIS AND CALCULATIONS

The design of a Miller OTA (Operational Transconductance Amplifier) involves careful analysis of each stage to ensure all MOSFETs operate in saturation, and the required gain, bandwidth, and biasing conditions are met. The OTA consists of a differential input pair, active load, current mirror, and an output gain stage. The following equations govern the operating points, biasing, and voltage levels across various nodes in the circuit.

P/V = 1m / 5V = 200 uA.

Iref = 30uA

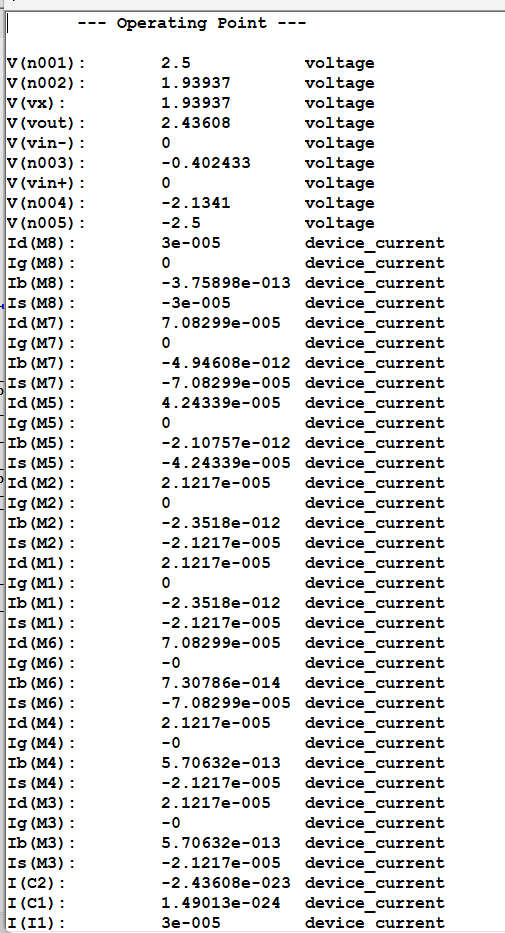
(W/L)1,2 =100u/500n

(W/L)3,4 =20u/500n

(W/L)5,7,8 =500u/500n

(W/L)6 = 100u/500n

DC ANALYSIS

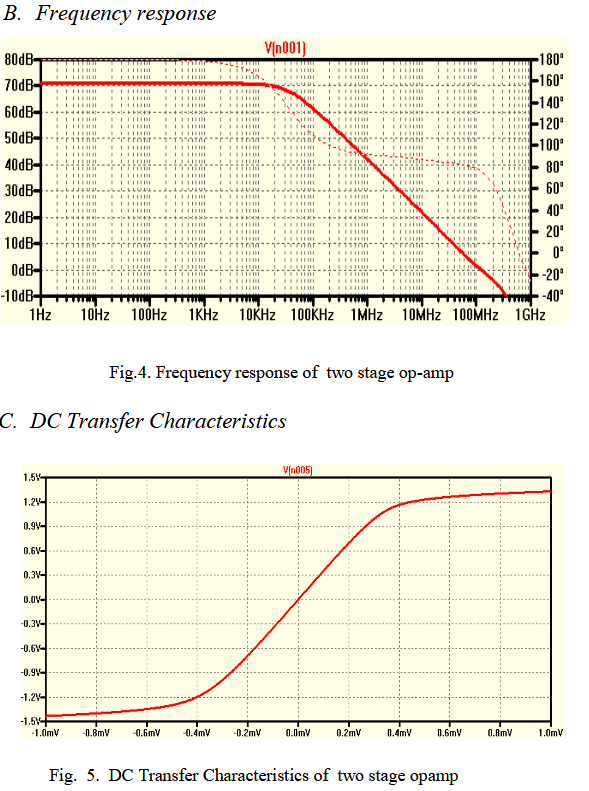
The DC operating point analysis of the Miller OTA was conducted to validate the stability and biasing conditions of each transistor in the circuit. The design ensured that all transistors operate in their saturation region, which is essential for proper amplification and linear behavior. During the DC analysis, the voltages across the critical nodes and the bias currents in each branch were thoroughly verified. observed during the simulation, confirming that the biasing network is functioning as intended. Additionally, the node voltages were within expected ranges to maintain saturation conditions and meet the desired input common-mode range (ICMR) and output swing.

# Equations Expected waveforms

# Expected results and specifications

AC Analysis (Gain and Phase vs Frequency):

Plot: Bode plot showing gain (in dB) and phase (in degrees).



Expected Output:

DC Gain: ~70 dB at low frequencies.

Unity-Gain Bandwidth (UGBW): 100 MHz (where gain = 0 dB).

Technology: 180nm CMOS

Supply Voltage (VDD): 2.5V

Target Gain: Greater than 60 dB

Phase Margin: Minimum 60° for stability

Gain –Band width product (GB) : Approximately 100 MHz

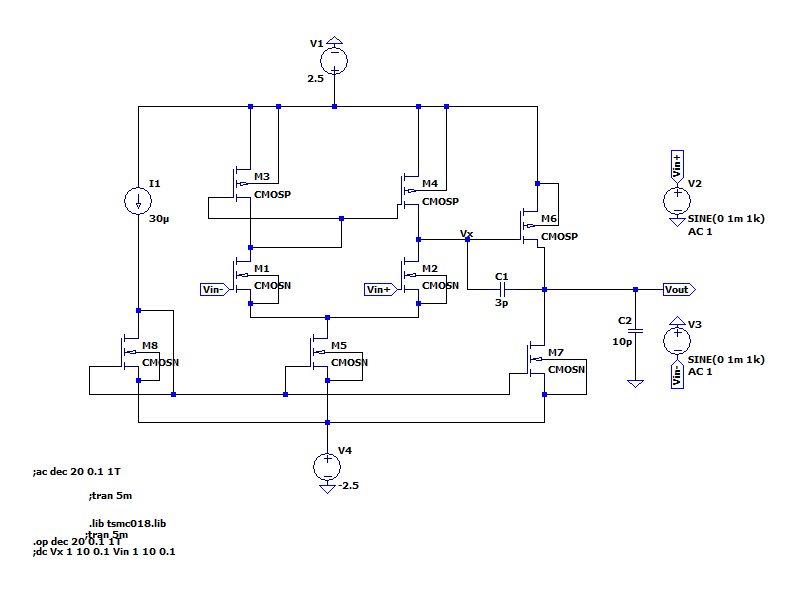
Load Capacitance: Between 1 pF and 10 pF

Compensation Capacitor (Cc): Tuned around 1–3 pF

Bias Current: Optimized for low power (~30 μA range)

Transistor Sizing: W/L ratios selected to balance speed and gain

SIMULATED CIRCUIT



CIRCUIT ARCHITECTURE

Two Gain Stages: The OTA uses two cascaded amplification stages to achieve high

overall gain.

Differential Input First Stage: The input stage (left side) amplifies the difference

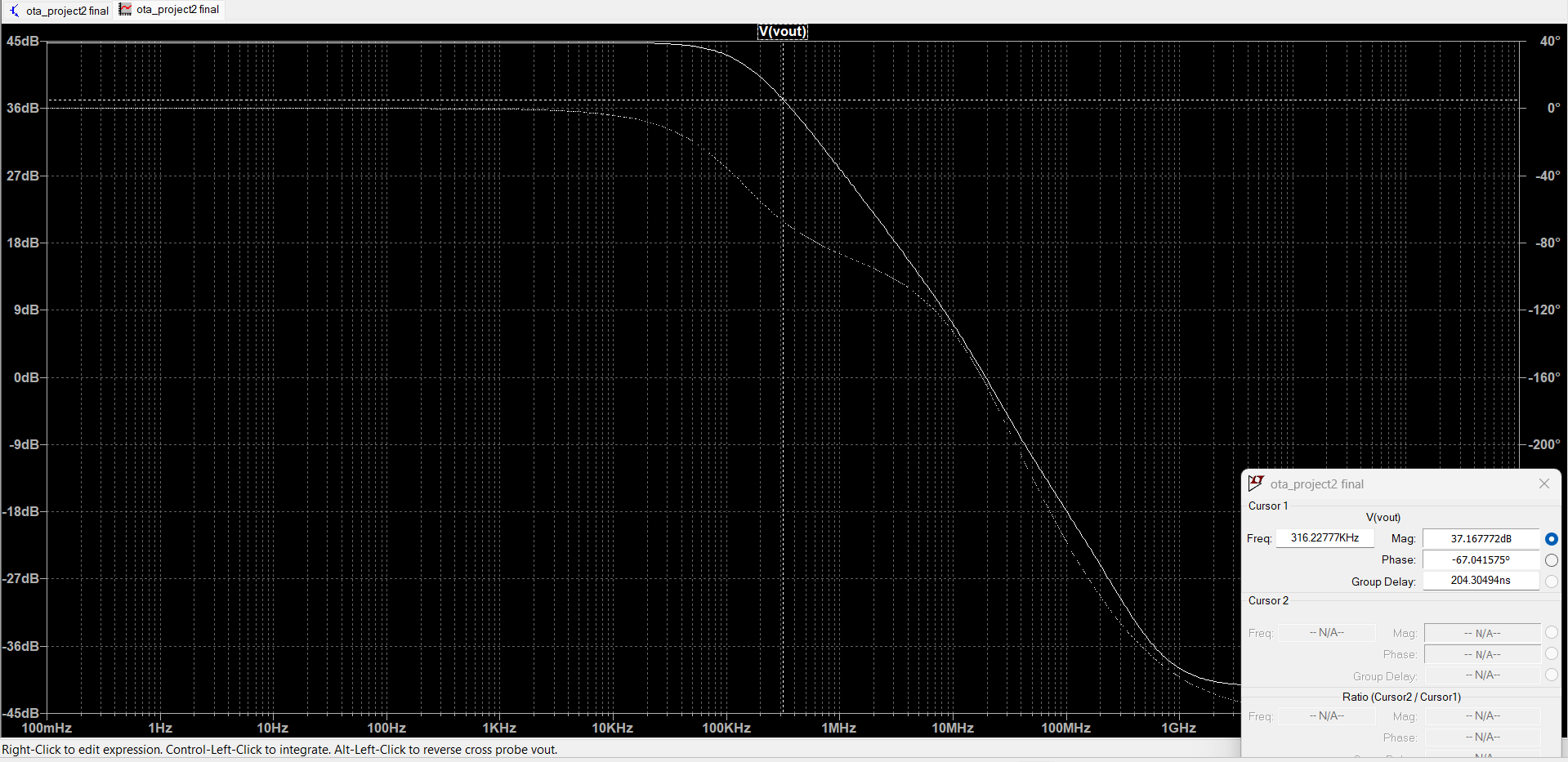
between the two input voltages.

Common-Source Second Stage: The second stage (right side) provides further

voltage amplification.

Miller Compensation (C1): A capacitor connected between the output and the input of the second stage stabilizes the amplifier.

Biasing Circuits: Dedicated circuits (like the one we discussed) ensure operation of both stages.

OBTAINED OUTPUT

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